## FPGA Verification System

The FPGA verification system consists of an image sensor, a LCD display and a PC running ISP turning tool. With this system, verification engineer can get real time image data from ISP or H264 which will improve work efficiency of ISP turning.



The following three daughter cards need to be made:

1. USB3.0 board is used for PC to access memories in SOC.
2. DPHY RX board is used for transfer DPHY signal to LVDS level.
3. DPHY TX board is used for LCD display with DSI interface.

## USB3.0 Board



## DPHY RX Board



## DPHY TX Board



## USB Communication Protocol

The turning tool shall obey this protocol when it get image through USB3.0. Each packet sent from PC has a header and payload. The header has 12 bytes and the maximum payload size shall less than 2M bytes.



Byte0: indicates write or read operation.

Byte1 ~ Byte2: reserved.

Byte3 ~ Byte7: operation address.

Byte8 ~ Byte9: total length of Head and Payload.